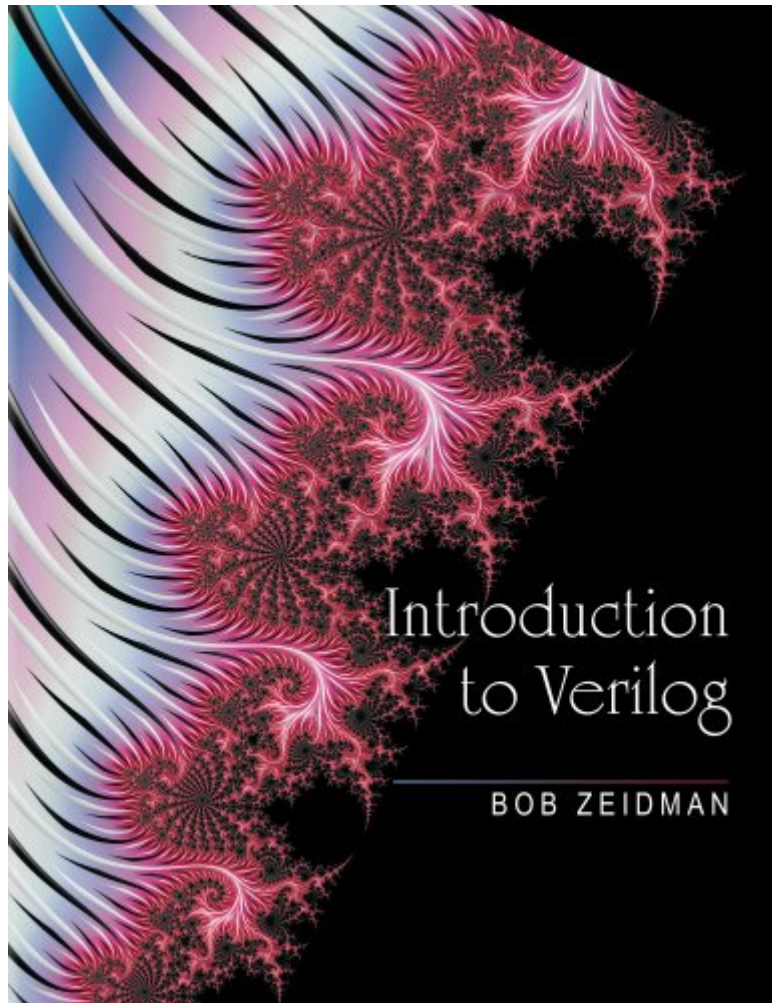




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# Introduction To Verilog



## Synopsis

This self-study guide came about as the result of the popularity of my textbook, Verilog Designer's Library. That book is an intermediate to advanced level reference book about the Verilog Hardware Description Language. Shortly after its publication, the Institute of Electrical and Electronics Engineers (IEEE) approached me to create an introductory book, based on the Verilog seminar that I give around the world. Over the years I've used the feedback from students to try to make it the best introductory Verilog course available.

## Book Information

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## Customer Reviews

If you are looking for a concise guide to help you learn how to write synthesizable Verilog to design and simulate real digital hardware in an FPGA, then this book is a very good place to look. I am a working FPGA application designer, published technical author, and part-time engineering professor, so my time is valuable to me -- the brevity and clarity of this book helps. If you understand the basics of digital logic at the schematic level and need to know how to design systems using Verilog HDL, then this should be a perfect fit for you. Anyone who's written this kind

of material would also appreciate the difficulty of explaining concepts like this, and the need for challenging the concepts with incremental "quiz" problems and practical application examples. As it says on the first page, the book is aimed at engineering students and working engineers who need to learn Verilog. If you would rather have a verbose, PhD thesis style coverage of the topic, look elsewhere and you'll find lots of them. To paraphrase Mark Twain and Blaise Pascal "It's much harder to write a short book than a long one." And it's \*much\* easier to criticize a work like this than it is to create one, so take the negative review here on with that in mind. I suspect that reviewer may be like some students who find it easier to blame the teacher rather than take responsibility for their own failings. If you are looking for a quick way to learn how to design digital systems using Verilog, then this book is a great place to start. And unlike some reviewers, I've never met the author and have nothing to gain or lose by my reviews, which is why I use my real name. Search for me on LinkedIn under kenarnoldentrepreneur if you have any doubts that this is a genuine review and I'm who I say I am. Cheers!

Im currently half way through the book. Im trying to teach myself Verilog on the daily subway commute. So far its informative, well laid out, and just a touch of humour to keep it going. The problem is the code listings are very poorly formatted in the kindle edition. I suspect its a factor of not having enough columns, which results in each original line spanning two or three lines in the kindle. Ive tried reducing the font and switching to landscape mode with limited results. As it is, it becomes impossible to follow the code listings or sample questions. I strongly request the author work on a kindle friendly edition. Cheers Rob

Be warned. If you intend to actually write Verilog code, do not buy this book. Of the 135 pages only 46 in fact provide new information. The rest is objectives, quizzes, final test, and answers to the quizzes and test. This is interspersed with supposedly humorous anecdotes. Concepts are introduced only to be explained much later. Want to review something you've read? There is no index or glossary of terms. The pages don't even show a chapter name. Not the kind of book to have by your side when actually designing and debugging code.

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